Novel Linearization Technique for Low-Distortion High-Swing CMOS Switches with Improved Reliability

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ABSTRACT
This paper proposes a linearization technique for low-distortion high-swing CMOS switches based on a new method of improving the linearity of the NMOS and PMOS conductances. This method has the advantage over conventional clock-boosting techniques of avoiding large gate voltages thus reducing the stress on the gate capacitance. Simulated results of a practical sample-and-hold circuit show that, using this technique, linearity levels compatible with 12-b can be reached over the Nyquist band.

1. INTRODUCTION
High-linearity switches are required in many low-voltage switched-capacitor (SC) circuits, spanning from 10-14b ADCs to accurate analog filters. As CMOS technologies continue to evolve towards lower supply voltages, new design techniques are needed to provide analog switches capable of rail-to-rail swings while exhibiting low-distortion. Furthermore, when requiring low-voltage operation, the reliability constraints of the technology have to be considered, avoiding over-stress of the CMOS devices due to large voltages being applied to the transistor gate. This paper addresses all these challenges by proposing a new linearization technique for low-voltage high-swing low-distortion CMOS switches with improved reliability. This paper is organized as follows. Section II describes the most relevant existing switch linearization techniques. Section III presents the proposed new technique and, in section IV, reliability improvement issues as well as simulated results are addressed. Finally, section V draws the main conclusions.

2. OVERVIEW OF EXISTING SWITCH LINEARIZATION TECHNIQUES

2.1. Conventional CMOS switches
Using CMOS technology a switch can be constructed by paralleling a NMOS and a PMOS device. The first advantage of having a CMOS switch rather than a single-channel MOS switch is that the dynamic analog signal range in the ON state is greatly increased as illustrated by the conductance curves in Fig. 1. Using a CMOS switch allows a full signal-swing. However, at low supply voltage operation, the equivalent switch conductance, $g_{EQ}$, has a large variation, which produces a large harmonic distortion in the sampled signal.

2.2. The Bulk-Switching Technique
The Bulk-switching technique (BS) [1] can be used to limit and reduce the variation of $g_{EQ}$. Fig. 2 shows a possible simple implementation of this technique where $M_1$ and $M_2$ are the main switches.

![Fig.1: NMOS, PMOS and equivalent ($g_{EQ}$) conductances versus input signal amplitude.](image1)

When the switch is ON, the bulk (N-well) of the PMOS transistor is connected to its source (by auxiliary transistors $M_3$ and $M_4$).

![Fig.2: Practical implementation of bulk switching technique.](image2)

This produces a lower threshold voltage value, independent from input signal level, since the body effect is reduced and, consequently, the conductance curve of the PMOS device is improved when comparing with the conventional CMOS solution as illustrated in Fig. 3. In the OFF state the bulk is then connected to $V_{DD}$ through the PMOS transistor $M_5$ increasing the OFF resistance due to the increased threshold voltage. This simple technique has been already successfully used in 12-bit ADC [2]. However, as shown by measured results in [2] and demonstrated by the simulated results in section IV, when using this technique the dynamic performance is highly degraded for high-frequency input signals. Moreover, the MOS switch is bidirectional and symmetric. The source and the drain terminals may
interchange depending on the input signal and on the previous sampled voltage. A latch-up problem can occur [3].

![Fig.3: Improved equivalent conductance (gEQ) of a CMOS switch with the bulk-switching technique versus input signal amplitude.](image)

2.3. Clock-Bootstrapping Circuits (CBTs)

To obtain constant-conductance operation the gate-to-channel voltage should be held constant during the ON state. This can be obtained using the bootstrap technique, which consists in boosting the gate voltage of the switch beyond the power supply voltage. In the OFF state the gate is grounded, the device is cut-off while a bootstrap capacitor $C_b$ is charged to $v_b = V_{DD}$. Then, in the ON state, this capacitor will act as a floating voltage source in series with the input signal making the gate voltage of the switch equal to $v_g = V_{DD} + v_{in}$, resulting in an overdrive voltage nearly constant over the input signal voltage range and, as a result, the switch’s ON conductance will be approximately constant and signal-independent.

A) NMOS version (CBTn)

Fig. 4 shows a possible implementation for an NMOS bootstrapped switch (CBTn) [4]. During the OFF state, switches driven by phase 2 ($S_4$ and $S_5$) are ON and the bootstrap capacitor $C_b$ is charged to $V_{DD}$. During the ON state, switches driven by phase 1 ($S_1$ and $S_2$) are ON and the resulting voltage is added to the input signal and applied to the gate of the main NMOS switch, $M_1$.

Critical switch $S_4$ has to be implemented with a NMOS device controlled by a bootstrapped signal from a charge-pump (CP), instead of being used a conventional PMOS with the source connected to $V_{DD}$ because, in that case, the switch could be turned ON during phase 1 due to the large voltage that occurs in the drain node (as high as $2V_{DD}$). Switch $S_2$ can be implemented by a PMOS, but leakage will occurs if the bulk is connected to $V_{DD}$. The bulk should be connected to its source or it may be necessary to connect it to $2V_{DD}$ from charge pump. Switch $S_5$, a NMOS, will support high voltage values, drain to source and gate do drain, and can be protected by adding a cascode NMOS device.

B) Improved PMOS version (CBTp)

Fig. 5 shows a possible implementation for an improved PMOS bootstrapped switch (CBTp) [5].

During the OFF state switches $S_4$ and $S_5$ are ON and, again, the bootstrap capacitor $C_b$ is charged with a voltage equal to $V_{DD}$. During the ON state (phase 1) switches $S_1$ and $S_2$ are ON, and the stored $V_{DD}$ voltage is added to the input signal and applied to the gate of the main PMOS switch, $M_1$. Capacitor $C_b$ is connected to the gate of $M_1$, and is charged between $2V_{DD}$ and $V_{DD}$ avoiding the need of an NMOS switch which would create a leakage current when the $M_1$ gate node voltage is highly negative. $S_2$ has to be implemented with a NMOS controlled by a CP circuit. In summary, this example combines the bootstrap gate control with the BS technique previously described. The bulk of the main switch $M_1$ is connected to the input terminal through $S_1$ when is ON, and to $V_{DD}$ through $S_3$ when it is in the OFF state.

C) Improved Conductances

As illustrated in Fig. 6, for both the CBTn and the CBTp circuits, the conductance of both switches becomes practically constant over the rail-to-rail signal swing (resulting in reduced distortion of the sampled signal).

![Fig.4: A NMOS bootstrapped switch (CBTn).](image)

![Fig.5: A PMOS bootstrapped switch (CBTp).](image)

![Fig.6: Improved NMOS and PMOS conductances versus input signal amplitude when CBT circuits are employed.](image)
However there are several drawbacks. First either for the CBThin or for the CBTip circuits there is a need of a CP circuit. On the other hand in clock-bootstrapping circuits there are always reliability issues that have to be taken into account as explained in previous paragraphs and in [4] (i.e. $V_{DS}, V_{GS}, V_{BS} \gg V_{DD}$), in order to overcome overstress and leakage problems, resulting in a highly complex circuit with many transistors. When compared with the CBThin circuit the CBTip version is better due to a reduction of the body effect in the main switch transistor.

3. PROPOSED NEW TECHNIQUE

3.1 Basic idea behind this new technique

Fig. 7 illustrates the idea behind the proposed linearization technique, which consists in improving the linearity of the conductance of both NMOS and PMOS switches by using two dedicated SC circuits, respectively, a n-type Switch-linearization circuit (SLCn) and a p-type Switch-linearization circuit (SLCp). The resulting equivalent conductance of CMOS switch becomes highly linear even for a rail-to-rail signal swing.

![Fig.7: Changes in the NMOS and PMOS conductances using the proposed technique versus input signal amplitude.](image)

The functionality of these two SLC circuits is described next for a NMOS switch (the following explanation is also valid for PMOS switch). When the device is ON and the input signal, $v_{ip}$, is close to $V_{SS}$, the SLCn block reduces the gate voltage, $v_{gn}$, that is applied to the NMOS switch to a value lower than $V_{DD}$. As a consequence its conductance is reduced. When $v_{ip}$ is close to $V_{DD}$, the SLCn circuit increases (boosts) gate-voltage $v_{gn}$ applied to the NMOS device, overcoming the zero-conductance problem of the NMOS transistors when having $v_{in} > V_{DD} - V_{th}$. The SLCn circuit generates an output gate-voltage to drive the switch approximately (neglecting parasitic effects) given by (1) where $C_{1n}$ and $C_{2n}$ are two small capacitors of a given size.

$$v_{gn} = v_{ip} \frac{C_{1n}}{C_{1n} + C_{2n}} + V_{DD} \frac{2C_{2n}}{C_{1n} + C_{2n}}$$

For the PMOS switch the analysis is similar and relatively straightforward as illustrated in Fig. 7. However, a slightly different linearization circuit, SLCp, is used to provide the suitable gate-voltage, $v_{gp}$, defined roughly by (2) where, again, $C_{1p}$ and $C_{2p}$ represent two small capacitors of a given size.

$$v_{gp} = v_{ip} \frac{C_{1p}}{C_{1p} + C_{2p}} + V_{DD} \frac{C_{2p}}{C_{1p} + C_{2p}}$$

Fig. 8 displays the conductance of both, NMOS and PMOS switches after linearization using the referred SLCn and SLCp circuits. As observed, the resulting equivalent conductance of the CMOS switch, $g_{EQ}$, is nearly constant.

3.2 Circuit Description and Practical Implementation

Fig. 9 displays two practical circuits that implement functions (1) and (2) conceptually (a) and in a practical implementation with real transistors (b).

![Fig.8: Improved equivalent conductance ($g_{EQ}$) of a CMOS switch when the proposed SLC circuits are used.](image)

![Fig.9: SLCn and SLCp circuits used for improving the linearity of main NMOS (M1) and PMOS (M2) switches. (a) conceptual SLC circuits; (b) practical SLC circuits.](image)
$C_{2n}$ to $V_{DD}$, and the other plate is pushed to a value lower to $2xV_{DD}$ because its charge is shared with $C_{in}$. Moreover, one plate of $C_{in}$ follows the input signal $v_{in}$ through switch $S_{in}$, being $C_{in}$ charge shared with $C_{2n}$. Function (2) can be explained in a very similar way. In the SLCn practical circuit $C_{in}$ and $C_{2n}$ are sized with 100fF and in the SLCp circuit the used capacitance values are $C_{lp}=C_{2p}=400fF$. Both, SLCn and SLCp circuits are optimized for a standard 0.18um CMOS technology with $V_{TN}=|V_{TP}|=0.5V$ and for a nominal supply voltage of 1.5 V. All NMOS and PMOS devices were respectively sized with aspect ratios of 1/0.18 and 4/0.18, except the main switches where (W/L)$_{M1}=10/0.18$ and (W/L)$_{M2}=40/0.18$ are used. This CMOS main switch was designed for a passive sample-and-hold circuit (S/H) comprising only the sampling switch and a 1pF sampling capacitor and capable of operation at a sampling-rate of more than 50MS/s. The SLC circuits can be scaled linearly for different sampling capacitors and different sampling-rates. Fig. 8 was already obtained from an electrical simulation of the practical circuit depicted on Fig. 9 (b).

4. SIMULATED RESULTS AND RELIABILITY ISSUES.

Fig. 10 displays the electrically simulated total harmonic distortion (THD) of a fully-differential passive S/H circuit, sampling at $F_s=50$MS/s, for the 5 different techniques described, for 4 different input signal frequencies (4.7, 11, 17 and 23 MHz) and for a differential input signal amplitude of 1Vpp. Circuits SLC, CBTn and CBTp are optimized using capacitors with the same total equivalent capacitance value.

As it can be observed, using the proposed SLC technique there is a significant improvement in the THD, especially for frequencies close to $F_s/2$, when comparing either with the conventional CMOS or with the BS technique. The achieved THD results are compatible with 12-bit linearity over the Nyquist band. On the other hand, it can be also verified in Fig. 10 that the THD results of the SLC solution are very close those obtained by the two CBT circuits. However, when reliability is taken into account the SLC solution is significantly better than the CBT ones. As illustrated in Fig. 11, the highest NMOS gate voltage, $v_{gn}$, is smaller than 2.05V (+137% of $V_{DD}$), and the smallest PMOS gate voltage, $v_{gp}$, is -0.65V (-43% of $V_{DD}$). In CBTn and CBTp solutions these values rise to about +167% and -65% of $V_{DD}$, respectively. Hence, the reliability is significantly improved using the new SLC technique over CBT solutions.

5. CONCLUSIONS

This paper presented a linearization technique for low-distortion high-swing CMOS switches based on a new method of improving the linearity of the NMOS and PMOS conductances. It was also demonstrated that gate stress voltages are reduced when compared with traditional CBT techniques, thus improving the reliability over existing clock-bootstrapping solutions. These two features make this technique more attractive than traditional clock boosting techniques for circuits requiring low distortion levels.

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